Abstract

An input signal with an associated pulse width can be sampled using a sampling method that does not require a clock signal. The input signal is compared to a reference level signal to produce a comparator output signal. Strobe signals are generated from the input signal, where the strobe signals occur within a pulse width of the input signal. Sampled data points are generated in response to the comparator output signal and the strobe signals such that the sampled data points are within the pulse-width of the input signal. One of the strobe signals may be used to periodically reset the comparator. The sampling logic circuit may be constructed from common logic gates and memory circuits such as flip-flops. In one example application the sampling method is applied to an equalizer system. The equalizer system includes an equalizer circuit that produces an equalized signal. A data slicer circuit converts the equalized signal into a digital representation. The sampling method is applied to the output of the data slicer circuit to generate the sampled data points in the equalizer system. The sampled data points may be used in the equalizer system or any other system that requires samples of the input signal without the use of a clock signal. Since the sampling system uses the incoming data signal to generate the requisite timing signals for sampling, high frequency clock circuits and phase locked loop techniques are unnecessary resulting in lower power consumption and reduced costs.